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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/118,359	07/17/98	KELLER J	MI22-587

021567
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MM42/0707

EXAMINER	
WHICHARD, G	
ART UNIT	**PAPER NUMBER**
2823	7

DATE MAILED: 07/07/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/118,359	Keller
Examiner	**Group Art Unit**
Glenn Whichard	2823

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-31* is/are pending in the application.

Of the above, claim(s) *15-24* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-14 and 25-31* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. The following title is suggested: Method of Forming Floating Gate Transistors for Enhanced Data Retention.

2. A substitute specification including claims is required pursuant to 37 CFR 1.125(a) because the holes punched in the pages, when the application was placed in the file wrapper, will render several words in the top line of each page nonlegible to the printer should the application be allowed. This does not affect the prosecution of the application .

A substitute specification filed under 37 CFR 1.125(a) must only contain subject matter from the original specification and any previously entered amendment under 37 CFR 1.121. If the substitute specification contains additional subject matter not of record, the substitute specification must be filed under 37 CFR 1.125(b) and must be accompanied by: 1) a statement that the substitute specification contains no new matter; and 2) a marked-up copy showing the amendments to be made via the substitute specification relative to the specification at the time the substitute specification is filed.

3. This application contains claims directed to the following patentably distinct species of the claimed invention: Species 1 is identified as the embodiment in which the methods for forming a floating gate transistor and enhancing data retention are primarily doping the

polysilicon layers. Species 2 is identified as the embodiment in which the methods for forming a floating gate transistor and enhancing data retention are based on control of the grain size and grain boundary area.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. During a telephone conversation with David Latwesen on June 18, 1999 a provisional election was made without traverse to prosecute the invention of species 1, claims 1-14 and 25-31. Affirmation of this election must be made by applicant in replying to this Office action. Claims 15-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(I).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

7. Claims 1, 2, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Shino (U.S. Patent Number 5,256,894). Shino discloses a method for forming a gate electrode (Fig. 1C and Column 3, Lines 23-53) substantially as recited including:

depositing a first polysilicon layer on a gate oxide layer on a silicon substrate;

the resistance of the first polysilicon layer is reduced by the inclusion of a high concentration of an impurity;

depositing a second polysilicon layer on the first polysilicon layer;

the second polysilicon layer has a lower impurity concentration than the first polysilicon layer.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shino (U.S. Patent Number 5,256,894) as applied to claims 1, 2, and 7 above, and further in view of Chou (U.S. Patent Number 5,272,099). Shino does not teach the relative thickness proportions

of the two layers. Chou discloses a method for forming a gate electrode with the thickness of a first polysilicon gate layer between about 500 to 800 Å (Column 2, Line 66) and a second polysilicon layer thickness between about 1500 to 3500 Å (Column 3, Lines 16-17). With these thickness ranges for the first and second layers:

the first layer can comprise at least 25 percent of the gate thickness and;

the first layer can comprise between about 25 to 75 percent of the gate thickness.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Chou regarding the layer thicknesses to the gate formation methods of Shino. One would have been motivated to do this to obtain the desired dopant levels and sheet resistance in the gate.

10. Claims 5, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shino (U.S. Patent Number 5,256,894) and Chou (U.S. Patent Number 5,272,099) as applied to claims 3 and 4 above, and further in view of Gardiner (U.S. Patent Number 4,354,309). Shino does not disclose values for the concentration levels of the dopants. Chou discloses a method for forming a multilayer gate electrode in which the first polysilicon layer is doped either in-situ or after deposition (Column 2, Line 62 - Column 3, Line 7) and the second layer is doped after deposition (Column 3, Lines 14-31). Gardiner discloses a graded multilayer polysilicon gate in which the dopant levels range from substantially zero for the first layer, to 10^{18} phosphorus atoms/cm^3 for the second layer, to 10^{20} phosphorus atoms/cm^3 for the third layer (Column 2, Line 54 - Column

3, Line 6). Thus, the individual polysilicon layers can be doped with phosphorus atoms in concentrations ranging from substantially zero to 10^{20} phosphorus atoms/cm^3. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Chou and Gardiner, regarding doping procedures and the range of concentrations that can be obtained, to the gate formation methods of Shino. One would have been motivated to do this to obtain the desired sheet resistance.

11. Claims 9, 10, 11, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shino (U.S. Patent Number 5,256,894), Chou (U.S. Patent Number 5,272,099) and Gardiner (U.S. Patent Number 4,354,309) as applied to claims 5, 6, and 8 above, and further in view of Yeh (U.S. Patent Number 5,840,607). Shino, Chou, and Gardiner do not explicitly disclose forming a dielectric layer over the multilayer polysilicon structure and forming a conductive layer over the dielectric layer. Yeh teaches a method for forming a floating gate in which an upper control gate, comprising a dielectric layer and a conductive layer, are deposited over the multilayer polysilicon lower gate layers (Fig. 4). The dielectric layer is a polyoxide, silicon nitride, silicon oxide sandwich structure with the oxide layers formed by thermal oxidation (Column 3, Lines 45-59). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yeh, for its intended purpose of forming an upper control gate, with the methods for forming a multilayer polysilicon gate disclosed by Shino, Chou, and Gardiner.

12. Claims 25, 27, 28, 29, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shino (U.S. Patent Number 5,256,894), Chou (U.S. Patent Number 5,272,099), Gardiner (U.S. Patent Number 4,354,309), and Yeh (U.S. Patent Number 5,840,607) as applied to claims 9, 10, 11, 12, 13, and 14 above. Shino, Chou, Gardiner, and Yeh do not explicitly disclose values for the sheet resistance of the polysilicon layers. The applicant discloses, on page 5 of the specification, an exemplary dopant concentration range of 10^{18} atoms/cm^3 to 10^{20} atoms/cm^3, and when phosphorus is utilized, the preferred sheet resistance is between about 600 ohm/sq. and 700 ohm/sq. It would have been obvious to one of ordinary skill in the art to perform a routine optimization exercise for the purpose of determining dopant concentrations required to form polysilicon layers with desired sheet resistance values as recited.

13. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shino (U.S. Patent Number 5,256,894), Chou (U.S. Patent Number 5,272,099), Gardiner (U.S. Patent Number 4,354,309), and Yeh (U.S. Patent Number 5,840,607) as applied to claim 25, 27, 28, 29, 30, and 31 above, and further in view of Hong (U.S. Patent Number 5,352,619). Shino, Chou, Gardiner, and Yeh do not disclose that the thickness of two layers of polysilicon can be substantially the same. Hong describes the formation of a floating gate (Fig. 4) in which the first polysilicon layer has a thickness of between about 500 to 1000 Å (Column 2, Lines 50-53) and the second layer of polysilicon has a thickness of between about 500 to 3000 Å (Column 6, Lines

13-16). Thus the two layers can have the same thickness. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Hong for its intended purpose, to the methods for forming a multilayer polysilicon gate disclosed by Shino, Chou, Gardiner, and Yeh.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Harada (U.S. Patent Number 4,143,178) discloses a method for forming multilayer semiconductor structures with doped polycrystalline layers. Nishimoto (U.S. Patent Number 5,814,543) discloses a method for forming a gate electrode using two layers of doped polycrystalline silicon.

15. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Glenn Whichard whose telephone number is (703) 308-4912. The examiner can normally be reached Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918. The fax numbers for this group are (703) 308-7722 and 7724 and 7382. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

George Fourson

Primary Examiner

Art Unit 2823

GW

G. Whichard

July 1, 1999